THORN
CONSUMER
ELECTRONICS

Single-Standard UHF
Colour Television

8000 Series

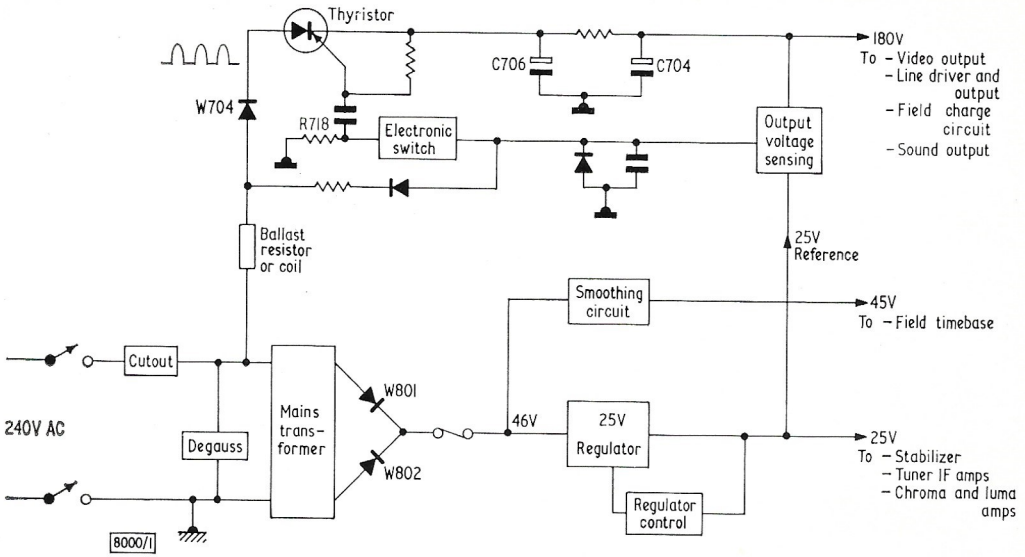
Circuit Description
(Including 8500 Chassis)

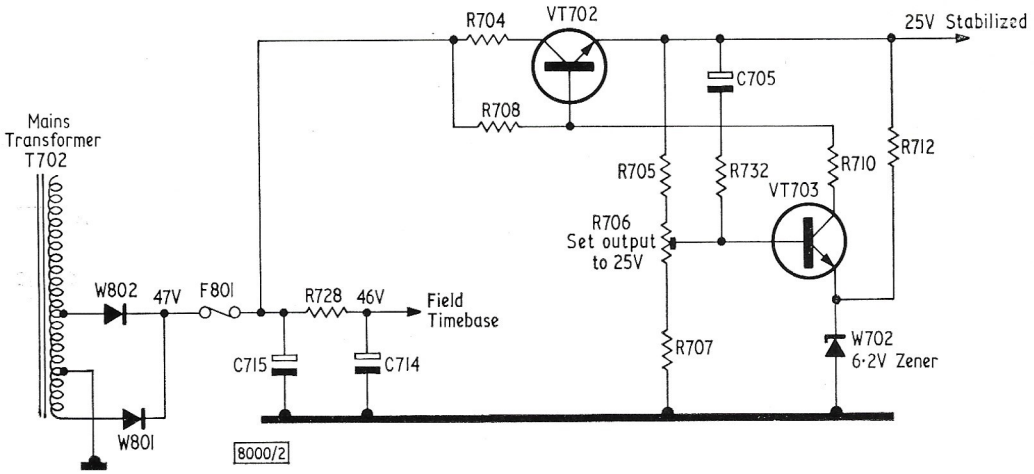
CONTENTS

POWER SUPPLIES

Contents

Note: For convenience, the high voltage rail is referred to as the 180V rail, although in practice the actual voltage may differ considerably from this figure.





46V Unstabilized and 25V Stabilized Supplies

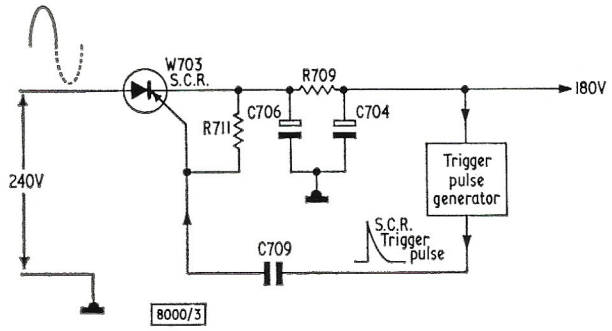
W801 and W802 form a full-wave rectifier supplying 47V unsmoothed to VT702, C715 being the reservoir capacitor. R728 and C714 are the smoothing components, and the resulting 46V unstabilized rail is used to supply the field oscillator and output stages.

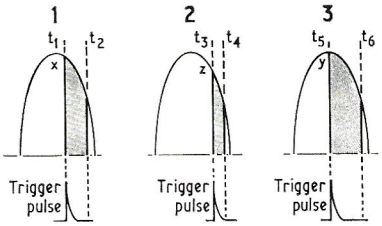
Emitter follower VT702 acts as a series regulator with the emitter voltage following the base voltage such that the emitter is at 0·5V *less* than the base (i.e. forward bias). If the base voltage increases, then the emitter voltage increases, and vice versa.

Initially R706 is adjusted to give 25V output at VT702 emitter. In setting up the receiver, this adjustment must be made first because it is used as a reference for the 180V supply (discussed later). VT702 base voltage (and hence the 25V output) is controlled by VT703 collector voltage.

VT703 collector voltage is controlled by VT703 base voltage since the emitter is clamped to 6·2V by W702.

VT703 base voltage will vary in proportion to changes in the 25V output supply. If, for example, the output supply voltage increases, VT703 base voltage increases; consequently VT703 collector voltage decreases, VT702 base voltage decreases and, finally, VT702 emitter voltage decreases thus counteracting the original increase. C705 and R732 couple any 100 Hz ripple in the output to the base of VT703 thus providing electronic smoothing.





Note: The S.C.R. always switches off when the anode volts fall below the cathode volts

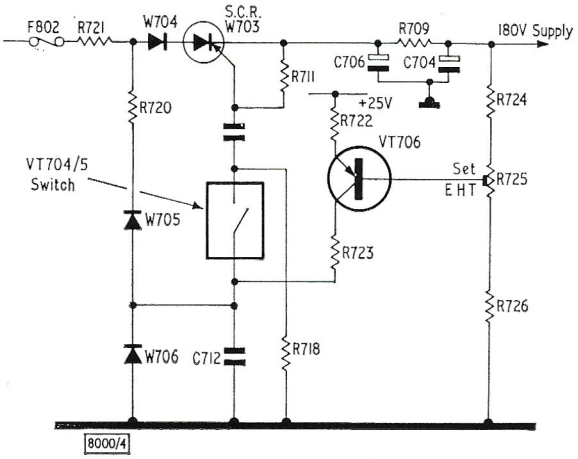
Basic Function of W703 (Silicon Controlled Rectifier)

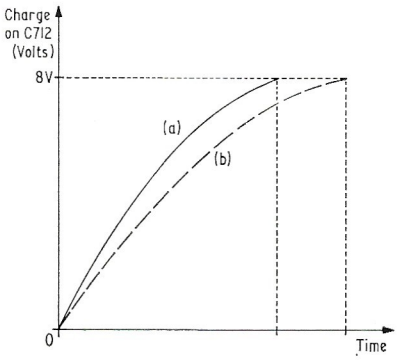
The SCR can start to conduct only when the anode is positive with respect to the cathode *and* a positive trigger pulse is applied to the gate. It will then continue to conduct, even if the gate pulse is removed, *until* the anode voltage falls below the cathode voltage, i.e. like an ordinary diode.

Whilst the SCR is conducting, the HT reservoir capacitor is being charged from the positive-going half-cycles of voltage. If the HT decreases, then the SCR is triggered earlier and stays on longer.

Consider three situations with reference to the illustrations above:

1. HT is correct. Assume that the trigger pulse switches the SCR on at point X and C706 is charged for the period (t_1———t_2).
2. HT is high. The trigger pulse switches the SCR on later in the half-cycle at point Z and C706 receives a charge for a shorter period (t_3———t_4).
3. HT is low. The trigger pulse switches on the SCR at an earlier point (point Y) and C706 is charged for a longer period (t_5———t_6).





180V Regulated Supply

W704 rectifies the mains feed such that only positive-going half-cycles are applied to the SCR W703, thus reducing the reverse blocking requirement of the SCR.

VT704-5 forms a switch which closes when the voltage across C712 reaches 8V at which point the SCR is triggered.

W705 and W706 conduct during the negative-going half-cycles of mains voltage, opening the switch and resetting the charge on C712 to just below chassis potential (voltage drop across W706 is approximately –0·7V).

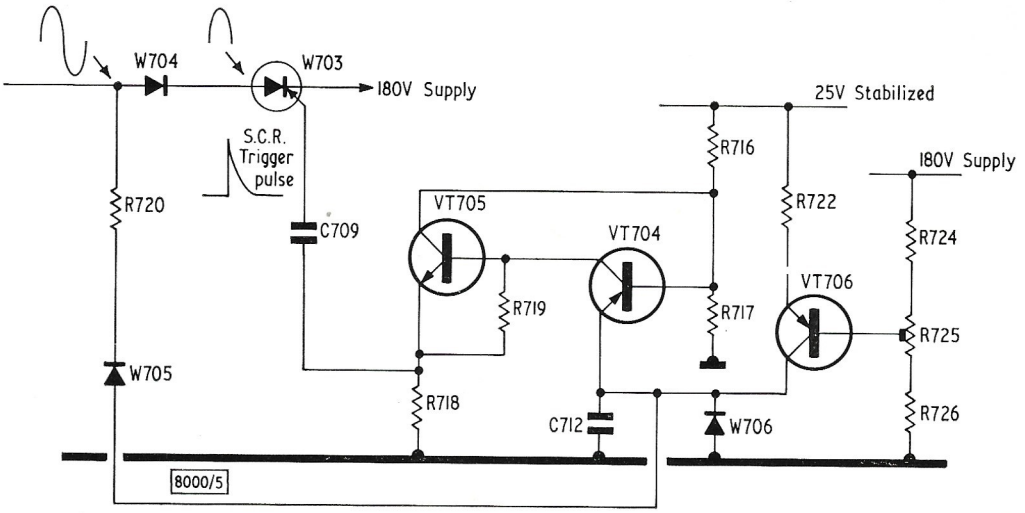
When the 25V supply is established, C712 is steadily charged up to 8V by the current through VT706.

The base of VT706 is referred to the 180V supply via the potential divider R724, R725 and R726. Variation in the 180V rail will produce a proportionate variation in the bias on VT706 base and hence in the charging current in C712.

The graph shows that the time taken for C712 to charge up depends on the voltage level on the 180V rail:

(a) 180V rail falls—VT706 base voltage falls causing increased conduction in VT706 thereby charging C712 up to 8V more quickly. Consequently, the SCR is triggered earlier in the half-cycle and the output rises to the correct level.

(b) 180V rail rises—VT706 base voltage rises reducing conduction in VT706 and slowing down the rate at which C712 charges up to 8V. Consequently, the SCR is triggered on at a later point in the half-cycle, feeding less current into the supply and causing the output voltage to fall to the correct figure.



Electronic Switch (VT705-VT704)

Switch Closing. When the charge on C712 reaches 8V, VT704 becomes forward biased and starts to conduct (since the emitter is now positive with respect to the base). VT704 collector current flows through R719 and R718 causing the base of VT705 (NPN) to go positive with respect to its emitter, thus turning VT705 on.

The effect of VT705 drawing current through R716 lowers the base voltage of VT704 driving VT704 on harder.

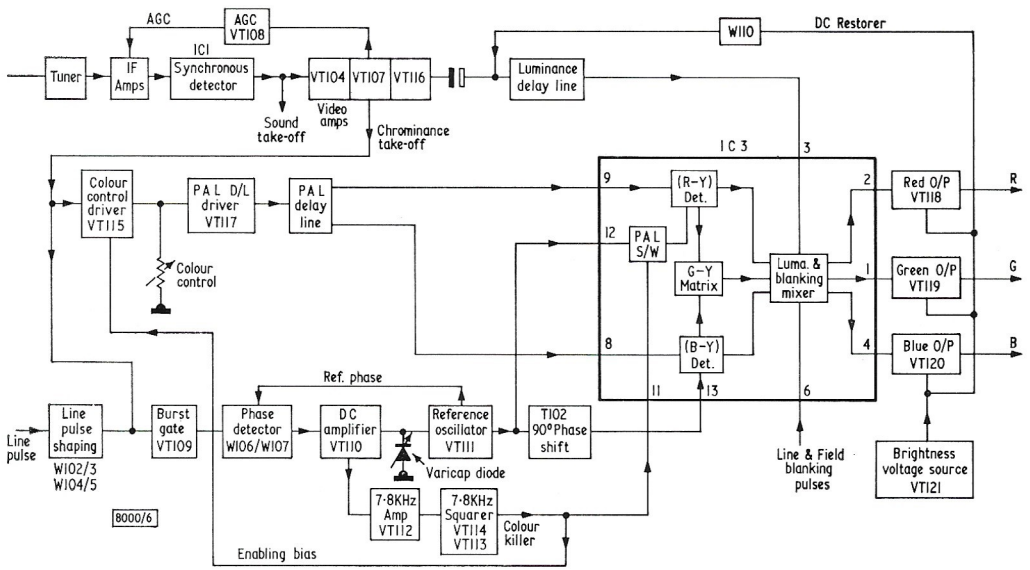
Regenerative action quickly switches both transistors hard on (switch closed) connecting C712 across R718 and producing an 8V positive-going pulse to trigger the SCR.

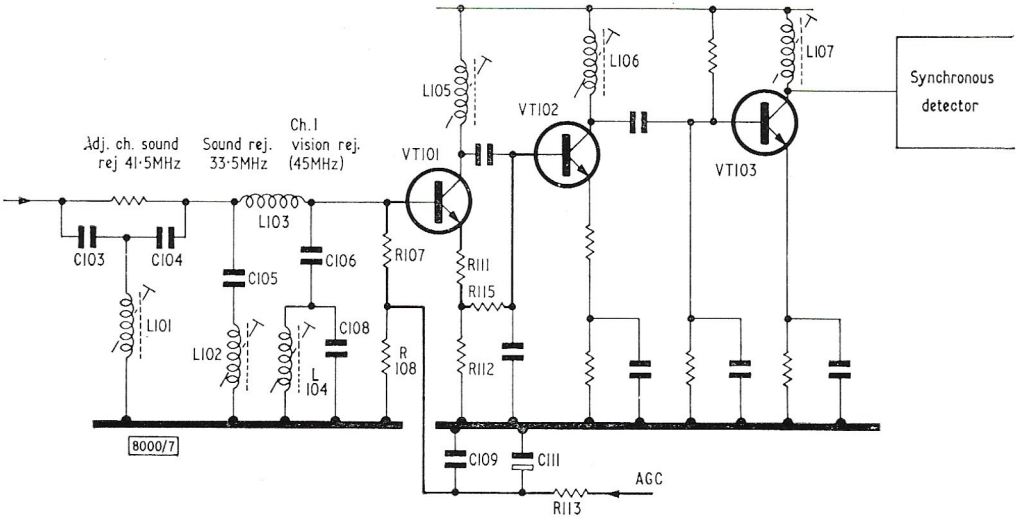
Switch Opening. The switch is opened, i.e. both transistors are turned off when C712 is discharged through W705-R720. This occurs when W706 and W705 conduct during the negative-going half-cycles of mains input voltage.

As C712 discharges, the emitter voltage of VT704 falls below the base voltage, switching off VT704 which in turn switches off VT705 (switch is now open). C712 begins to charge again on completion of the negative-going mains half-cycle and the process is repeated.

SIGNAL CIRCUITS

Contents



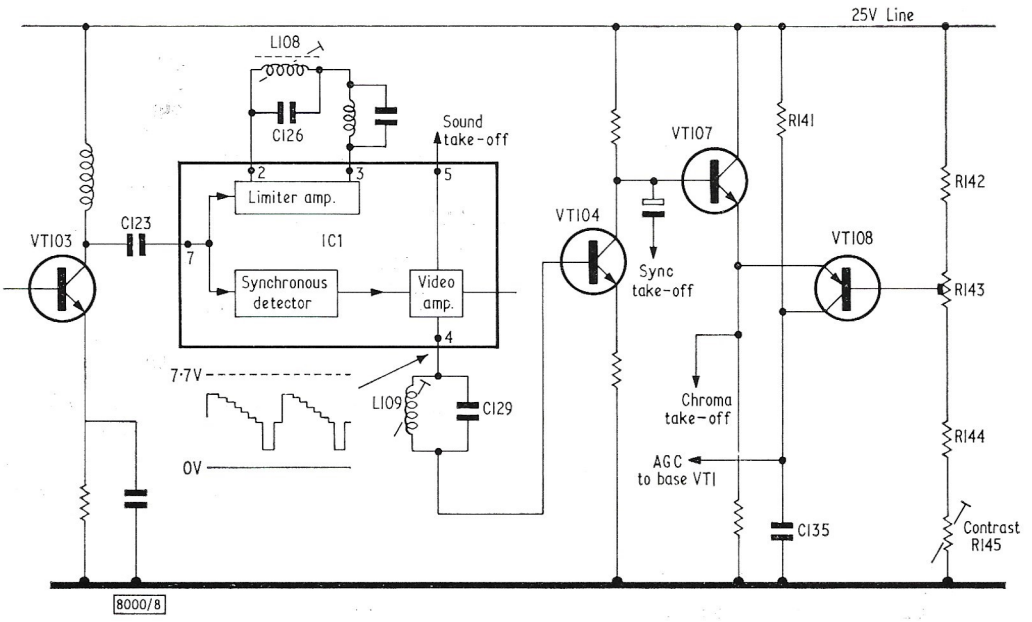


Vision IF

The majority of the IF filtering is carried out in the base circuit of VT101. C103, C104 and L101 form an adjacent channel sound rejector (41·5 MHz). Approximately 18 dB of rejection is provided at the sound carrier frequency (33·5 MHz) by C105 and L102, whilst L104, C106 and C108 comprise a rejector at the channel 1 vision carrier frequency (45 MHz).

VT101, VT102 and VT103 form a three-stage broadly tuned IF amplifier with stagger tuning which is employed to achieve the correct response. VT101 collector circuit is tuned to 38·9 MHz, VT102 is tuned to 34 MHz, and VT103 is tuned to 37 MHz. The vision carrier position and response bandwidth is set by fine adjustments of L105 and the tuner coupling L103, whilst any tilt can be corrected by small changes in the setting of L107 from its nominal 37 MHz position.

The first IF stages are AGC controlled, the control bias being applied to the base of VT101 via R107 from the filter network R113, C109 and C111. The sense of the AGC is positive-going for gain reduction. The base of the second stage receives its control voltage via the emitter of the first stage. The signal amplitude at the input to the synchronous detector (IC1) is 30-50mV.



Synchronous Detector and AGC

Synchronous Detector. The IF signals from VT103 collector are applied to pin 7 of IC1 and thence in parallel to the synchronous detector and the limiter amplifier within the IC. The limiter amplifier and external tuned circuit L108-C126 are used to extract the vision carrier component which is then applied as a reference signal to the synchronous detector section of the IC which is also fed with the amplitude modulated carrier. The reference carrier performs a switching action within the detector such that it inverts one half of each modulated cycle, and the resultant output is a negative-going video component which is amplified before being fed out at pin 4. At this point the video signal is negative-going towards 0V from a no-signal level of +7·7V, i.e. as the signal input to the IC increases, the DC at pin 4 decreases.

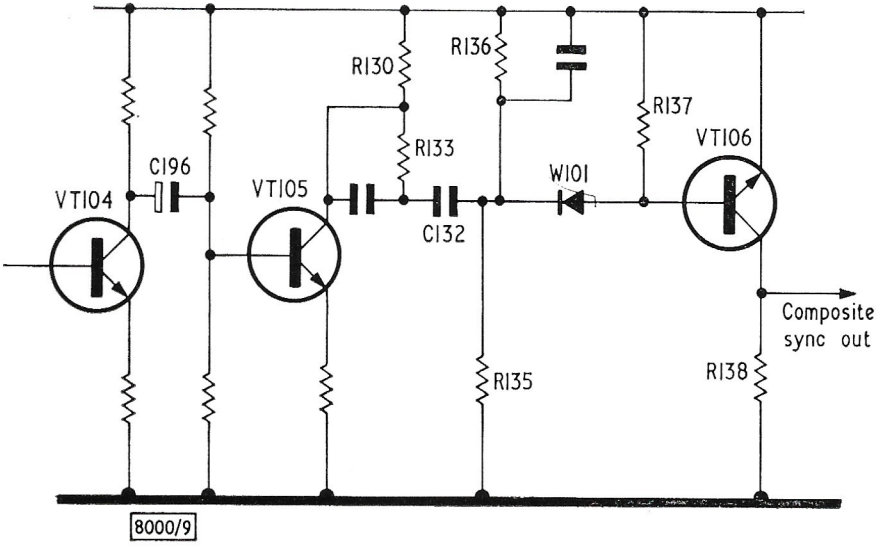
A practical test of availability of video at pin 4:
Aerial out–Pin 4 reads 7V DC (approx.).
Aerial in–Pin 4 reads 5V DC (approx.).

A video signal of the opposite polarity appears at pin 5 and is fed via a ceramic filter to the intercarrier sound demodulator.

AGC. From pin 4 of IC1, the video signal is fed via the 6MHz rejector circuit L109-C129 to the invertor stage VT104. The DC output from the IC provides forward bias for VT104.

The inverted signal at the collector of VT104 drives the emitter follower VT107 which has the AGC driver VT108 coupled to its emitter. R141 with R113 and R108 (not shown) forms a potential divider which sets the bias on the first two stages of the IF amplifier. With no signal input these stages are biased for maximum gain and VT108 is cut off by the reverse bias obtained from R142, R143, R144 and R145.

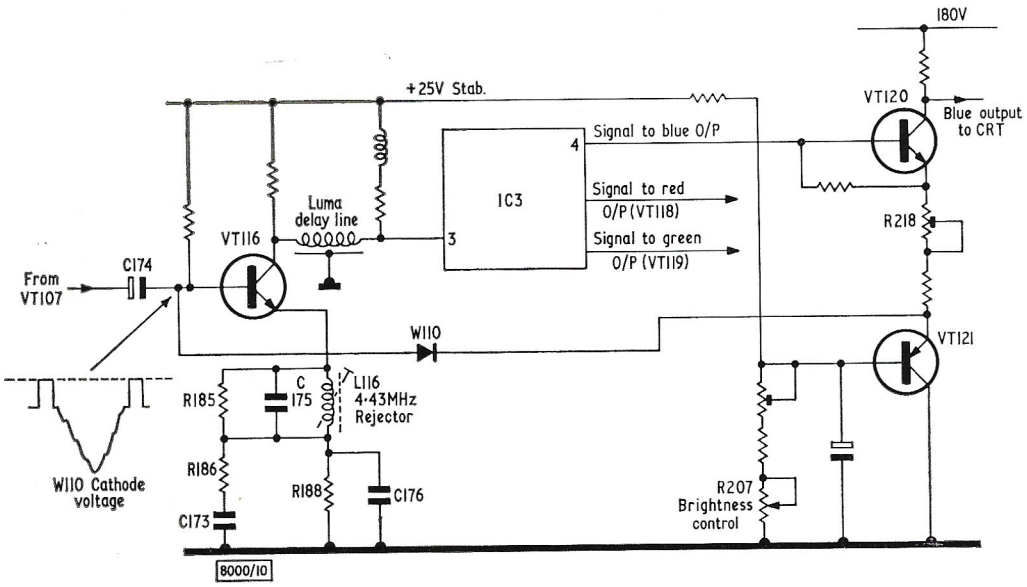
During reception, the positive-going sync pulses appearing at VT107 emitter cause VT108 to conduct on the tips of the sync pulses and the collector current charges C135 which is sufficiently large to smooth out line frequency information. The charge on C135 causes an increase in the voltage applied to the first two IF stages (increased voltage with increasing signal level). Heavier conduction in the transistors lowers the gain. Manual adjustment of the gain is provided by R143 and R145.



Sync Separator

The signals present at VT104 collector are AC coupled to the buffer stage VT105 where the polarity is again inverted for correct operation of the sync separator VT106. Negative-going sync pulses cause W101 and VT106 to conduct. The current flowing in C132 during conduction alters the charge on this component. The potential divider R135 and R136 provides a higher impedance path whereby the charge on C132 can recover partially between sync pulses.

During this recovery period, the cathode of W101 is positive with respect to its anode and diode action protects VT106 against reverse base-emitter voltage Due to phase reversal in the transistor, positive-going composite sync pulses appear across R138 in the collector and are fed to the timebases.

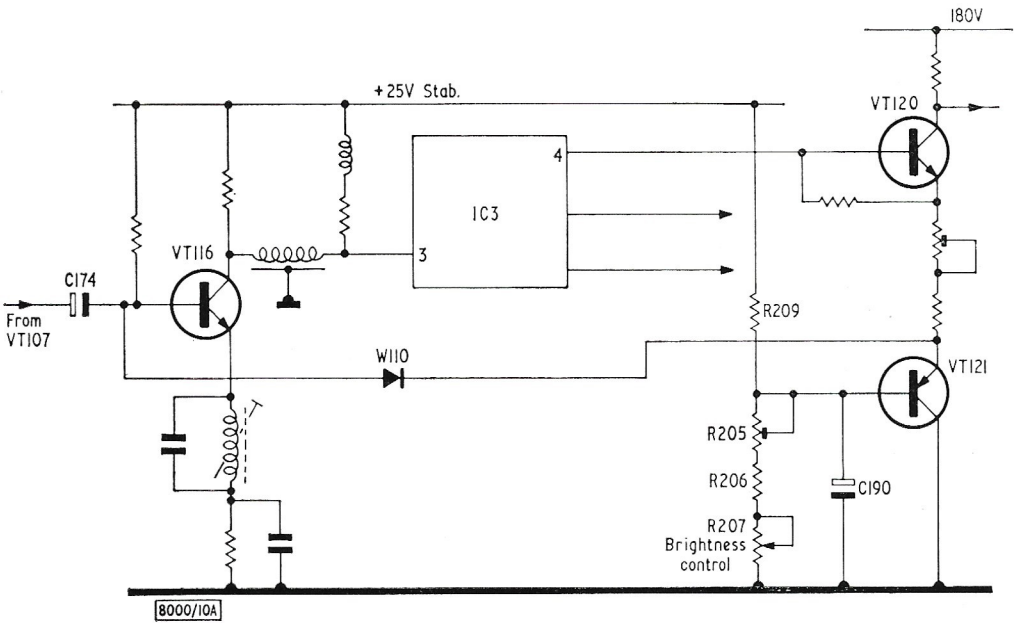


Luminance Signal Path

The signal present at the emitter of VT107 is fed to the chrominance bandpass circuits (dealt with at a later stage) and via C174 to the luminance amplifier VT116. A subcarrier rejector is introduced in the emitter (L116-C175) to reduce the visibility of chroma patterning. The rejector is damped by R185 to restrict the depth of the notch to about 6dB.

Emitter compensation is provided by R186, C173 and R188 which give a lift in the response at 1·2MHz to compensate for a corresponding dip in the colour processing IC (IC3) through which the luminance signal passes. Further correction to the overall response is provided by C176 which gives increased lift at the higher luminance frequencies.

After passing through the luminance delay line and being processed in IC3, the R, G and B signals appear at the output pins and are applied at the bases of the three video output stages which in turn drive the cathodes of the CRT.

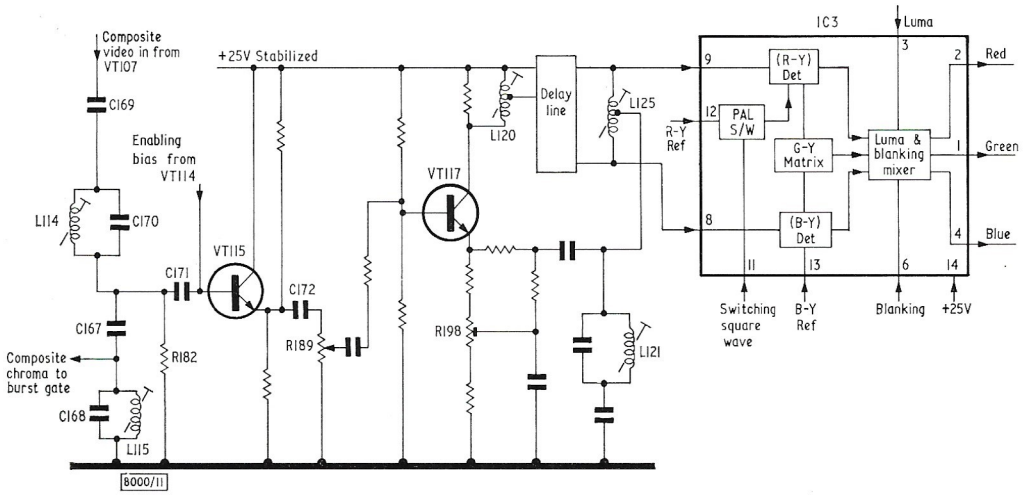


DC Restoration and Brightness Control

DC restoration is provided by W110 which conducts on the sync pulse tips and alters the state of charge on C174. This DC restoring potential is obtained from the Brightness control emitter follower VT121.

The Brightness control voltage is obtained from a potential divider R209, R205 (Brightness) R206 and R207 connected between the 25V stabilized rail and chassis. This voltage is applied at the base of VT121 which is connected in the emitter return of the three video output transistors. The voltage at the base of VT121 is negative-going for increased brightness, i.e. as VT121 conducts harder, the emitter voltage falls; consequently the three video output emitter voltages fall causing increased conduction in the video output transistors. As a result, the video output collector voltages are reduced and this reduction is communicated to the CRT cathodes which are negative-going for increased brightness. The fall in VT121 emitter voltage is also communicated to VT116 base via W110 (DC restorer) causing VT116 collector voltage to rise. This increase is passed to the bases of the three video output transistors via IC3, resulting in a further increase in brightness, i.e. additive to the change caused by the reduction in the output emitter voltages.

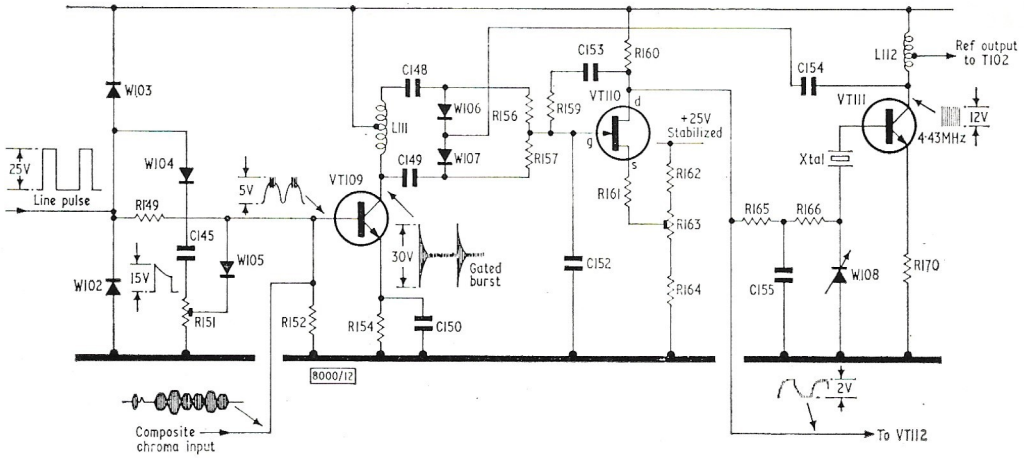
Note: Due to the DC loop via W110, any DC change caused by a fault condition in VT116, IC3 or in the output stages will affect all DC conditions in these stages, e.g. W110 goes open-circuit–VT116 base voltage rises, and the collector voltage falls, resulting in insufficient DC input to IC3 via pin 3; consequently the amplifiers in IC3 are cut off and there is no luminance or colour output.



Chrominance Channel

VT115 is turned on during colour transmission by the 'enabling' bias from VT113 and VT114. The video signals at VT107 emitter are applied via C169 to the bandpass network in VT115 base. The network includes a 6 MHz intercarrier rejector L114-C170 and a 4·43 MHz acceptor circuit L115-C168 which is tuned to accept the chroma signal with a 2 MHz bandwidth. The resulting signal is applied via C171 to the base of VT115. VT115 is connected as an emitter follower to provide a low impedance for the colour control R189 which provides adjustment of the level of signal applied to the delay line driver VT117.

The output of VT117 (approximately 600mV) drives the delay line. The direct (undelayed) signal is taken from the emitter. R198 in the emitter allows adjustment of the stage gain to proportion correctly the direct and delayed signals. L121 adjusts the phase of the direct signal. The direct signal is now injected at the centre tap of the delay line terminating coil L125, and by a process of addition and subtraction the R-Y component appears at one end and the B-Y at the other. Each component is then applied at the appropriate input of the demodulator and mixer IC3.

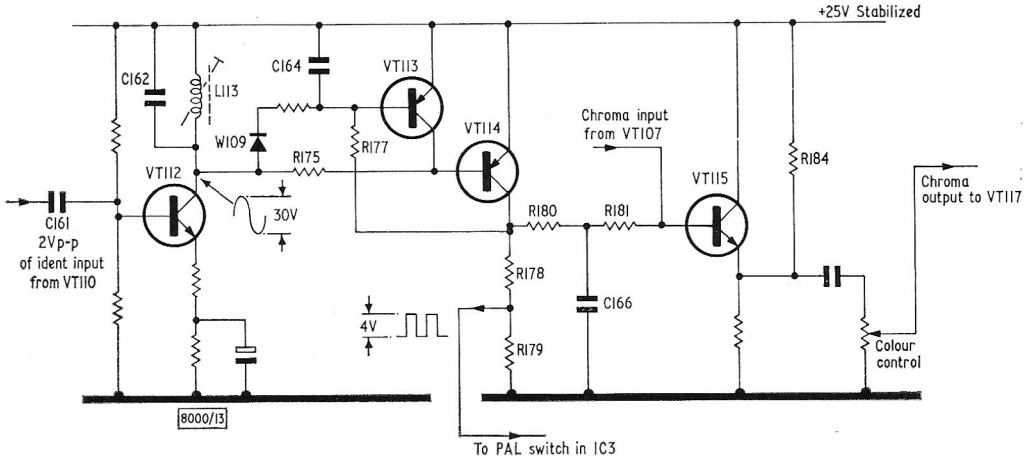


Burst Gate and Phase Discriminator

VT109 is switched on during the burst period by a positive-going delayed line flyback pulse. The line pulse is applied across W102 and is clamped between the 25V line and chassis by W103 and W102 respectively. After attenuation by R149 and R152, the line pulse appears at the base of VT109 together with the chroma and burst signal fed in via C151. At the same time the 25V pulse switches on W104, and C145 is charged via R151. The time constant of C145-R151 is such that the voltage across R151 rises and then decays to a point where its value is lower than the pulse voltage on VT109 base. At this point, W105 conducts and cuts off VT109. This point is adjustable by means of R151 which is set such that VT109 cuts off at the conclusion of the burst. VT109 is held off during the active line period by the charge in C150 holding the emitter positive with respect to the base until the next line pulse arrives.

The amplified burst appearing at VT109 collector is applied in opposite phase across the discriminator diodes W106-W107 with the reference oscillator signal being applied to the centre of the diodes. Output voltage from the discriminator (appearing across C152) contains the error voltage to correct the oscillator phase/frequency and also the ident signal (ripple) due to the swinging burst.

The error information is applied to the high impedance FET DC amplifier VT110. Assuming the reference phase lags the burst, then the error voltage will make VT110 gate more negative; consequently the drain goes more positive, increasing the reverse bias on varicap diode W108 to reduce its capacitance and the reference oscillator speeds up and locks on to the burst phase. R163 is adjusted initially to set up the reference oscillator phase/frequency. By means of this correction loop the oscillator is maintained in quadrature with the average burst phase. The averaging is carried out by the filtering of C153-R159 together with the filtering action of C153-R159 together with the storage circuit R165-C155 which prevents sudden changes in oscillator frequency due to the intermittent nature of the burst. The oscillator is a conventional circuit, the sub-carrier being selected in the collector by L112 and fed out to the demodulator via T102.



7.8kHz Amplifier, Colour Killer and PAL Switch Driver

As the burst swings alternately ±45deg. about its nominal phase, a square-wave at half-line frequency is produced at the output of the phase detector. After amplification in VT110, this AC component is fed via C161 into the base of VT112, and develops a 30V p-p sine-wave across the tuned circuit L113-C162 in the collector.

The positive-going half-cycle of this sine-wave is rectified by W109, charging C164, the bottom plate going sufficiently positive to bias off VT113.

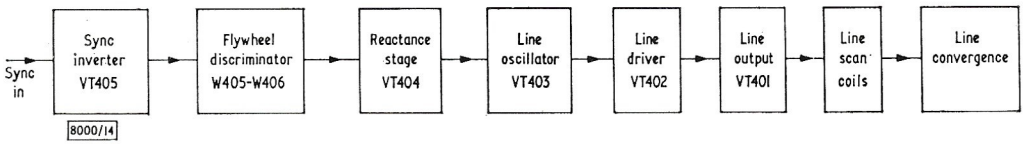
The large amplitude 7·8kHz sine-wave is also fed to VT114 base. It saturates VT114 on negative-going half-cycles and cuts it off on positive-going half-cycles, yielding a square-wave output at the collector. The square-wave output is attenuated by R178 and R179 to about 4V p-p making it suitable for operation of the PAL switch in IC3.

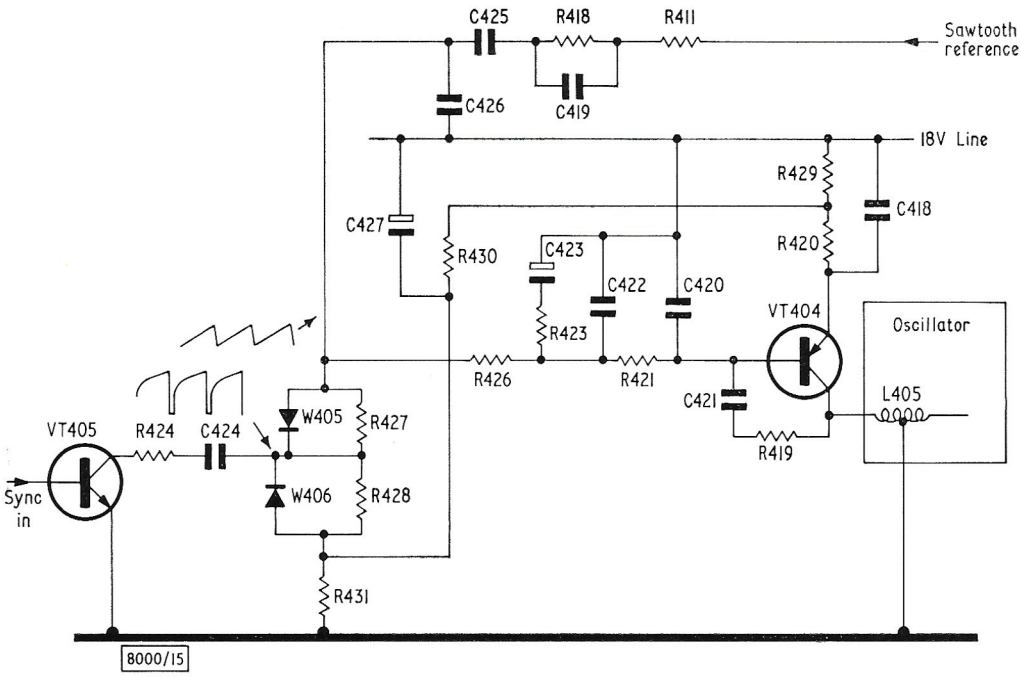
The square-wave is also passed through a low-pass filter R180 and C166, where its DC component (approximately 13·5V) is extracted.

This voltage is the 'enabling' bias which is used to switch on the colour control driver VT115 during colour transmissions. In the absence of a colour signal, no 7·8kHz waveform will be produced because of the missing burst. As no charge is applied to C164, the current through R177 causes VT113 base potential to fall below the emitter potential and VT113 is turned on. VT113 collector voltage rises and VT114 base voltage rises, turning VT114 off. VT114 collector voltage falls to about 3V and therefore there is insufficient bias to drive the colour control driver VT115, and the chroma channel is muted.

LINE TIMEBASE and CONVERGENCE

Contents



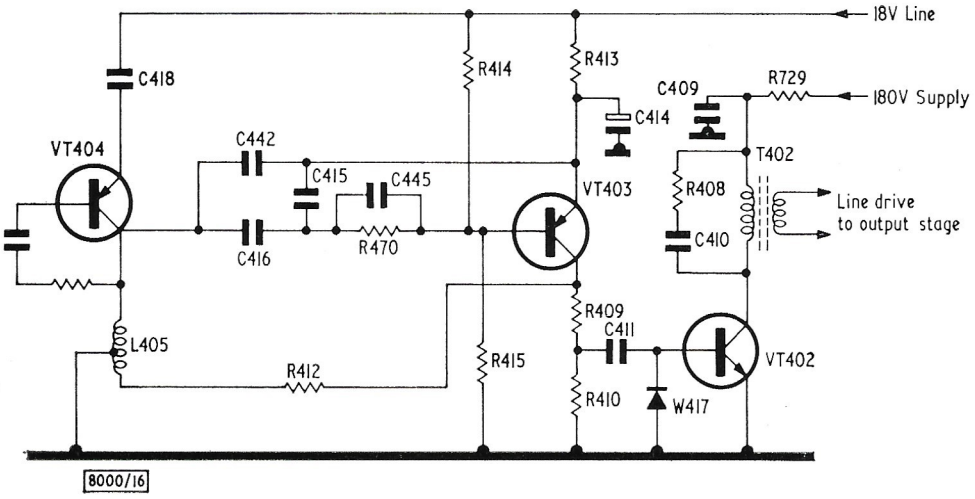


Flywheel Discriminator and Reactance Stage

Line Flywheel Discriminator. A sawtooth reference derived from a winding on the line output transformer is applied to the flywheel discriminator W405-W406 via integrator R411-C426 and DC blocking capacitor C425. R418 and C419 in parallel provide phase adjustment ensuring that the discriminator gives zero output when the picture is correctly centred and all other settings are normal.

After inversion in VT405 the negative-going syncs are applied as gating pulses at the junction of the discriminator diodes. The discriminator circuit yields an output which is related to the phase difference between the sync pulse and the sawtooth reference, thus providing the control bias required to keep the oscillator in step with the sync pulses. The output from the discriminator is filtered by C423, R426 and C422 and applied to the base of the reactance stage VT404.

Reactance Stage. The reactance transistor is connected in shunt with the oscillator circuit between L405 and C418. A phase-retarded fraction of the collector voltage is developed at the base by R419, C421 and C420. After phase inversion due to transistor action in VT404, the result is a 90deg. lag in the current with respect to the voltage in the transistor, thus creating the effect of an inductive reactance across the oscillator. Any change in VT404 base bias due to flywheel action will alter the value of this inductance and thereby pull the oscillator back to the centre frequency.



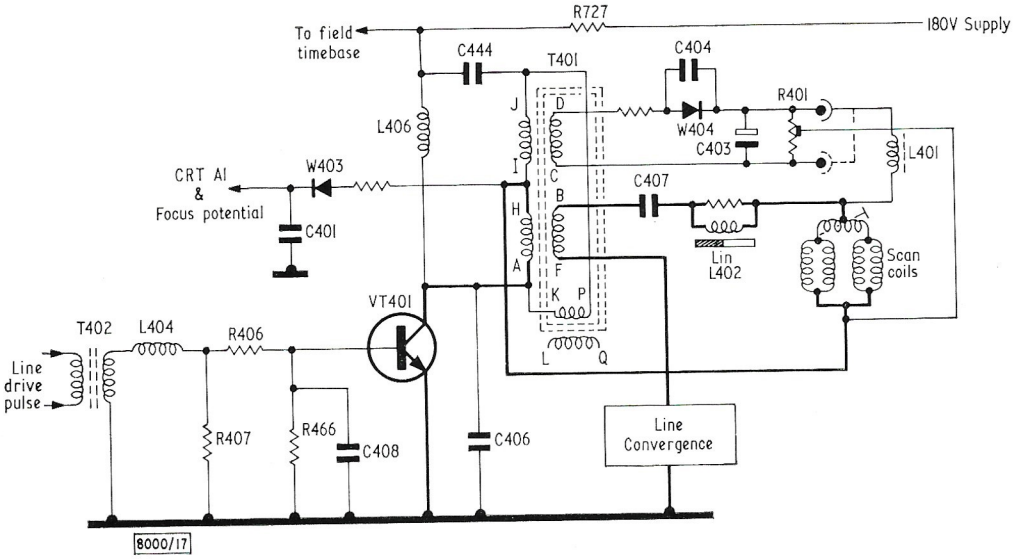
Line Oscillator and Line Driver

The oscillator circuit comprises L405 which is tuned by C416, C415 and C442 together with the inductive reactance of VT404. C442 has a negative temperature coefficient characteristic and is chosen to compensate for the thermal characteristics of the other components. The conduction time of VT403 (26μS approximately) is determined by C445 in parallel with R470.

Positive feedback between collector and base of VT403 is via R412, L405 (which introduces a phase reversal) and the capacitive tap formed by C416 and C415.

The largely square waveform developed across R410 is fed into the base of the driver transistor VT402 via C411 with DC restoration provided by W417.

The line driver VT402 operates from the 180V rail via R729. The square wave at the base is amplified and developed across the primary of T402. R408 and C410 are connected across the primary of T402 to damp any high voltage spikes caused by leakage reactance in the transformer.



Line Output Stage

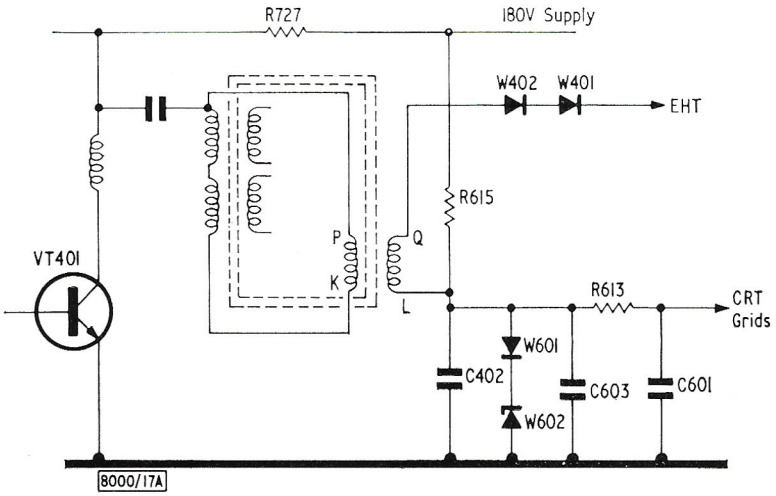
Line Output. The following notes deal with the 8000 Series line output stage. Basic operation of the 8500 is similar; differences are dealt with on page 39.

The line output transistor is switched on and off by the pulses received from the driver transistor via T402. Collector HT is obtained via R727 from the 180V regulated supply. The primary windings of the line output transformer (AH, IJ and FB) have equal numbers of turns so that the scan coils are coupled to the collector of VT401 with a 1 : 1 turns ratio. This arrangement ensures that the large value scanning voltages are balanced to chassis to reduce radiation and allows the line convergence current to be taken from the low potential end of the circuit at point F. Tuning capacitor C406 determines the duration of the positive-going flyback pulse by resonating the parallel combination of the scan coils and T401 primary.

At the end of the forward scan stroke, VT401 is cut off and the energy stored in the scan coils flows into C406. This energy starts to oscillate due to the back EMF developed, but on the negative half-cycle the collector base junction of VT401 conducts allowing a linear decay of the current through the scan coils thus producing the first part of the scan (i.e. the collector-base junction performs as an efficiency diode). Before this current reaches zero, VT401 is switched on again to complete the remainder of the scan. Note that the switch-off time at the base is delayed by L404 to allow the removal of charge carriers accumulated at the collector junction. R406 limits the base current. The base-emitter junction is protected against flash-over pulses by C408, and R466 damps the input circuit against ringing. C407 is the 'S' correction capacitor and L402 is a saturable inductor which provides linearity correction.

The pulse waveform developed across winding DC is rectified by W404, smoothed by C403 and fed via R401 as shift current to the scan coils. L401 isolates the shift circuit from the scan circuits.

The potential for the CRT A1 and focus electrodes is obtained from W403 which rectifies the pulse waveform appearing at junction IH.

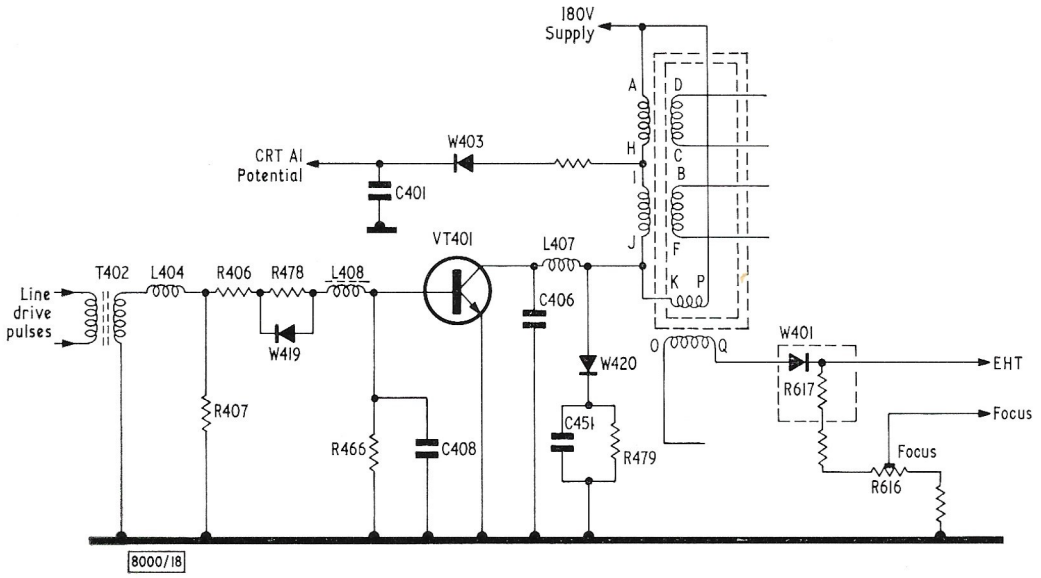


EHT and Beam Current Limiting

EHT. Third harmonic tuning is employed in the EHT overwind which generates the EHT voltage of 22kV (25kV in 8500) directly to feed the silicon rectifiers W401-W402. The length of the lead carrying the 22kV to the EHT rectifier is critical to the tuning of the overwind.

The collector feed resistor R727 is deliberately undecoupled to give width stabilization. As beam current is drawn, tending to increase the width, the increased current through R727 results in a lower voltage at VT401 collector, thus opposing the original tendency towards overscan. The voltage at the low potential end of R727 is also fed to the field timebase to provide similar stabilization for picture height. A further function of R727 is to limit the peak current drawn by VT401 in the event of CRT flashover.

Beam Current Limiting. The low potential end of the EHT overwind is decoupled by C402 and C603, and is returned to chassis via the diode combination W601 and W602. The diodes are also connected via R615 to the 180V supply, and a bias of 27V for the CRT grids is developed from this supply across the zener W602. This corresponds to a current of 1mA flowing through the diodes in opposition to the overwind current. If the beam current exceeds the permitted figure (approximately 1mA) the bias from the 180V line is overridden and the CRT grid voltage moves in a negative direction, thus opposing the increase in beam current. W601 is included to prevent the CRT grid being clamped to chassis potential as W602 becomes forward biased. Filtering of the grid bias is performed by C603-R613-C601 with C603 also maintaining grid voltage for a short period after switch-off to prevent spot persistence.



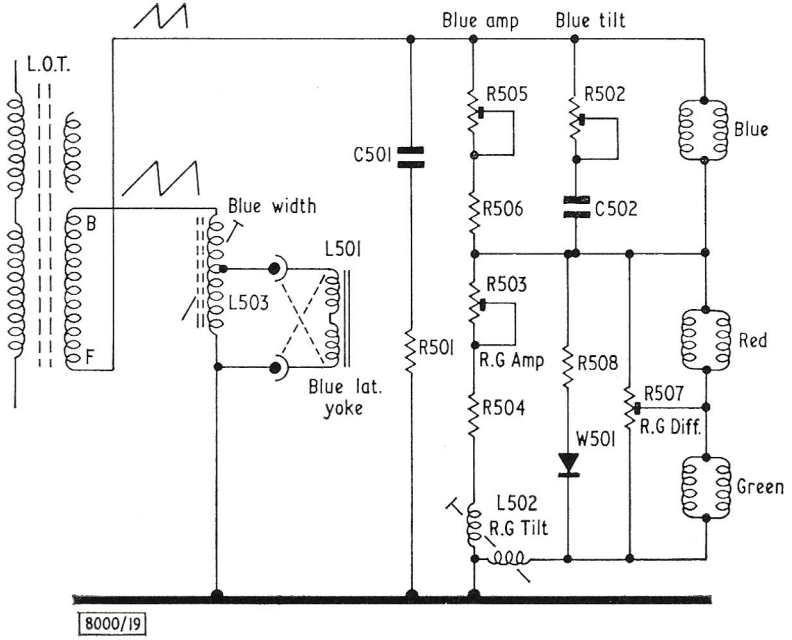
8500 Series Line Output Stage

Basic operation is similar to that already described for the 8000 Series, but the 8500 Series employs a different type of transistor with higher current gain and current rating (not interchangeable with the 8000 Series).

R478 is included in the base circuit to reduce the level of drive in the *on* condition, whilst L408 modifies the rate of charge carrier extraction at the collector junction during the *off* period. W419 bypasses R478 during the switch-off phase so that the effect of L408 is not reduced by the presence of series resistance.

Protection for VT401 against voltage surges, particularly on flashover, is provided by the network W420-C451-R479. These components may not be fitted in some early chassis. When fitted, they will be found attached to the plastic moulding which houses the desaturation winding L406 in the 8000 chassis. (Due to the high current capability of the 8500 Series line output transistor, the desaturation choke is not required.)

Other differences in the 8500 Series line output stage include different turns ratio for higher EHT (25kV) and the derivation of the higher focus potential from a potential divider connected across the EHT.



Line Convergence

The line convergence circuit forms a low impedance network in series with the scan circuit. The red and green controls are matrixed but separate controls are used for the blue adjustments. C501 and R501 are connected in series across the convergence circuit to ensure that the convergence circuit appears substantially resistive to the line output stage.

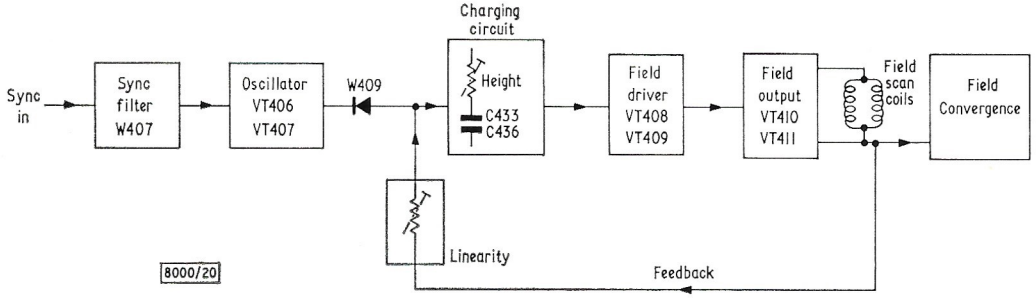
L503 provides a series or shunt inductance with the blue lateral coils for integration of the 600V sawtooth pulse from point B on the line output transformer. The connector for the blue lateral coil is reversible to allow correction to be applied in either direction; it can also be disconnected if no correction is required.

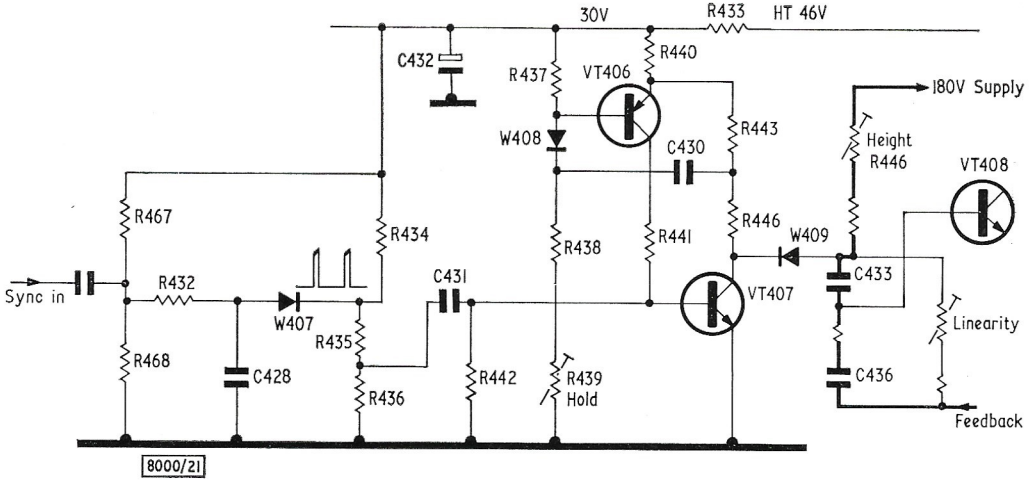
Line scan current flowing in R503, the R.G. Amp control, produces a sawtooth voltage which drives a parabolic current through the red and green coils permitting adjustment at the left-hand side of the screen. Adjustment of the sawtooth component is provided by L502 (R.G. Tilt) which allows adjustment at the right-hand side of the screen. The proportionate level of parabolic current in the red and green coils is adjusted by R507 (R.G. Difference) and the same function is provided for the sawtooth component by the Line Scan Balance control L403 (not shown). W501 clamps the sawtooth to prevent static shift being caused by dynamic adjustments and also reduces interaction between the Amp and Tilt controls.

The level of the mainly parabolic current flowing in the blue radial convergence coils is determined by the setting of R505 (Blue Amp). The parabolic component is increased by the presence of C502 to a degree determined by the setting of R502 (Blue Tilt).

FIELD TIMEBASE and CONVERGENCE

Contents





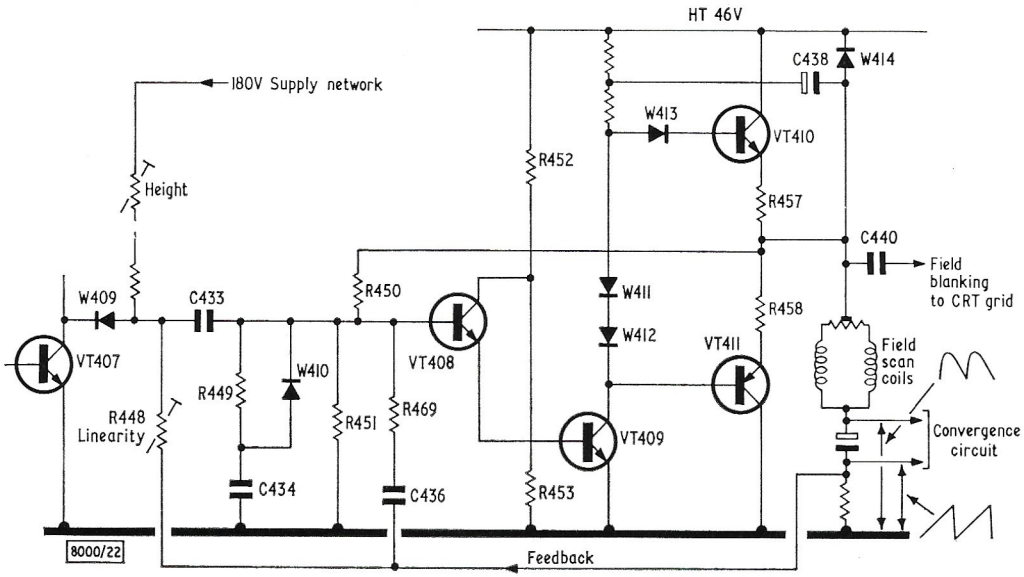
Sync and Oscillator

Field Sync. Field sync is separated by the integrator R432-C428, the resultant positive-going pulse being coupled into the base of VT407 via W407 and C431. In the absence of a sync pulse, W407 is reverse biased by the network which includes R434, R435 and R436. The arrival of the pulse initiates flyback.

Field Oscillator. VT406 and VT407 form a complementary relaxation oscillator. During scan, both transistors are non-conducting due to the large positive charge on C430 which reverse biases W408 and consequently raises VT406 base above its emitter. VT407 is non-conducting due to the lack of forward bias at its base. During this period the field charging capacitors C433 and C436 are being charged from the 180V supply, via the Height control R446, to produce the linear scan voltage. VT407 is isolated from the charging circuit by W409 which is held off by the full decoupled HT appearing at its cathode.

Flyback. The positive charge on C430 leaks away via R438 and R439 (Vertical Hold) at a rate which is determined by the setting of the Hold control. Assuming the oscillator is free-running, i.e. no sync pulses, then a point is reached where W408 is switched on by the fall in its cathode voltage, resulting in a reduction of VT406 base voltage which turns VT406 on. Conduction in VT406 causes an increase in its collector voltage which is communicated to VT407 base, turning VT407 on. From this point the complementary pair are driven hard on by regenerative action. Under normal operating conditions the transistors are turned on by the arrival of the sync pulse (prior to the initiation of switch-on by the discharge of C430 as described above).

With VT407 conducting during flyback, W409 cathode voltage falls, W409 conducts and the field charging capacitors are discharged through W409 and VT407. Meanwhile, C430 is being charged from the supply via R440, *e-b* junction of VT406, W408, R444 and VT407. As C430 approaches full charge, the voltage on VT406 base rises to a point where it exceeds the emitter voltage, causing VT406 and consequently VT407 to be cut off. C433 and C436 begin to charge again to provide the next scan stroke.



Sawtooth Generator and Output

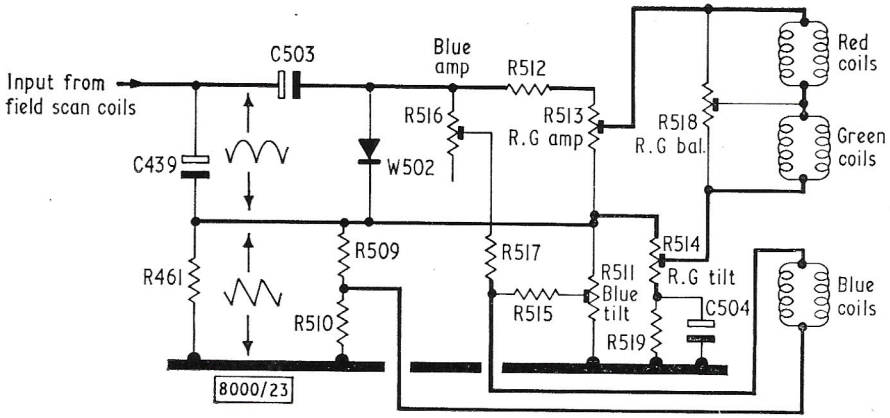
At the beginning of scan, VT408 and VT409 are off (due to C433 and C436 being discharged by W409-VT407). With VT409 in the *off* condition its collector is at 46V approximately and therefore VT411 (PNP) is off and VT410 (NPN) is hard on, driving current through the scan coils to produce the first half of the scan stroke. This current starts at maximum (top of picture) and decreases in a linear manner as C433 and C436 are charged up, progressively turning on VT408 and VT409 until, as centre of scan is approached (centre of picture) VT410 is almost turned off and VT411 starts to conduct, driving a linearly increasing current in the reverse direction through the scan coils to complete the scan.

Heavy negative feedback from the output stage is applied via C436 to ensure linearity. W410, R449 and C434 provide 'S' correction, some of the initial input current to VT408 base being diverted into C434 to slow down top of scan.

The bottom portion of the scan is slowed down by the normal fall-off as C433 and C436 approach full charge. W410 discharges C434 on flyback to reset the circuit.

W411-W412 ensure that both output transistors are conducting at centre of scan to prevent crossover distortion.

At the beginning of flyback, W409 discharges C433 and C436, cutting off VT408 and VT409. VT411, which was conducting during the latter half of the scan, also cuts off, and the sudden change in current through the scan coils results in a positive back e.m.f. appearing on the anode of W414. As this rises to the same potential as the supply rail, W414 conducts, clamping the scan coil voltage at this level as current flows into the supply line, until this current falls to zero. During this phase, VT411 is held off by C438 which communicates the positive excursion to its base. C438 also supplies VT410 base current as VT410 conducts in reverse during flyback.



Field Convergence

The field convergence waveforms are obtained directly from the field output stage. The sawtooth current in the field scan coils develops a sawtooth voltage across the sampling resistor R461 and a parabolic voltage across the coupling capacitor C439.

The parabolic voltage appears across R513 (Amplitude control) and the sawtooth across R514 (Tilt control). The matrixed red and green convergence yoke coils are connected between the sliders of these two controls. Differential drive to the red and green coils is provided by the R.G. Difference control R518, whereas tilt balance is provided by R460 (R.G. Balance) connected across the input to the scan coils. C503 isolates the DC voltage in the scan coils from the convergence coils. Diode W502 acts as a DC restorer for the parabolic voltage across R513 and R512 but is deleted in later chassis on the introduction of R519 and C504 which provide some extra differentiation for the R.G. Tilt adjustment, giving increased effect of this control near top of scan.

The mainly sawtooth correction required by the blue gun is provided by the Blue Tilt control R511 which gives control in both directions by reason of the blue coils being returned to the junction of R509 and R510. The small parabolic component required is supplied via the blue amplitude control R516.

THORN
CONSUMER
ELECTRONICS

Thorn Consumer Electronics Limited

284 Southbury Road
Enfield Middlesex

Service Depots

LONDON PO Box 121 Edmonton
London N18 3BP

MANCHESTER Thorn House Derby Street
Cheetham Manchester 8

GLASGOW 155 Shieldhall Road
Glasgow SW1

THORN *A member of the Thorn Group*

1073S

01P1-725